SENSYLINK Microelectronics

(CA9555)
Low Voltage 16-bit I²C and SMBus I/O Expander with Interrupt

CA9555 is a 16-bit remote GPIO expander. It provides remote GPIO expansion for most MCU families via the I²C or SMBus interface.
It is ideally used in Server and Telecom equipment.

1. Description

The chip is a 16-bit I/O expander. It provides remote GPIO expansion for most MCU families via the I²C or SMBus interface. The CA9555 has two 8-bit Input Port register, Output Port register, Configuration register (setup as input or output), and Polarity Inversion register (active high or active low). After power on, the 16 I/O pins are configured as inputs with an internal weak pull-up to Vcc. However, the master can enable the I/O pins as either inputs or outputs individually by setup the configuration register bits. If no external signals are applied to the CA9555 I/O pins, the voltage level is high due to the internal pull-up resistors. The data for each input or output is stored in the corresponding input or output port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register.

The master can reset the chip probably caused by timeout or other improper operation using the power-on reset feature, which resets all registers in their default state and initializes the I²C/SMBus state machine. The chip has outputs latch feature, which can protect the chip when driving LEDs directly with high-current capability.

The CA9555 open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

Available Package: TSSOP-24, QFN4x4-24 package.

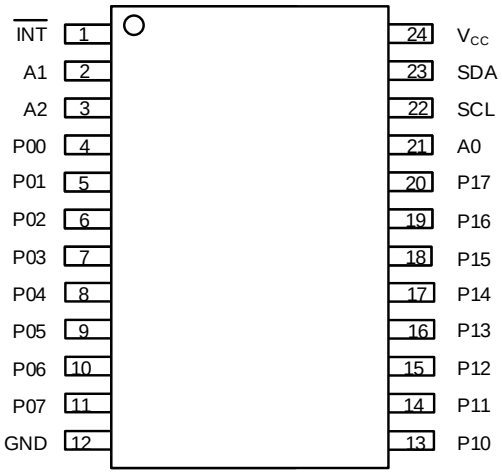
2. Features

- Operation Voltage: 1.65V to 5.5V
- Standby Current: 3.5μA (Max. 5.5V)
- 5.5V Tolerance I/O Port
- Remote 16-bit GPIO Expander
- Compatible with SMBus and I²C interface
- I²C Speed up to 1.0MHz (Fast-mode Plus)
- Up to 8 slave addresses
- Open-drain Interrupt output with active low to indicate input state changed.
- Input, Output, and Configuration Register
- Polarity Inversion Register
- Built-in Power-on Reset
- No Glitch during Power-up
- Noise Filter on SCL/SDA inputs
- 16 I/O pins
  - As Input with internal 100k pull-up resistor (default)
  - As Output with internal push-pull
- Latch feature when driving LEDs directly with high current capability
- Temperature Range: -40°C to 85°C

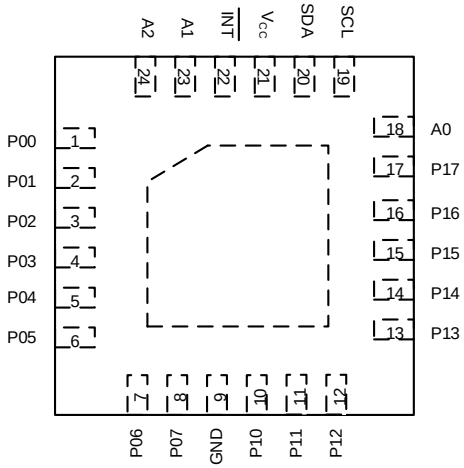
3. Applications

- Server, Notebook PC
- Telecom equipment

4. PIN Configurations (Top View)

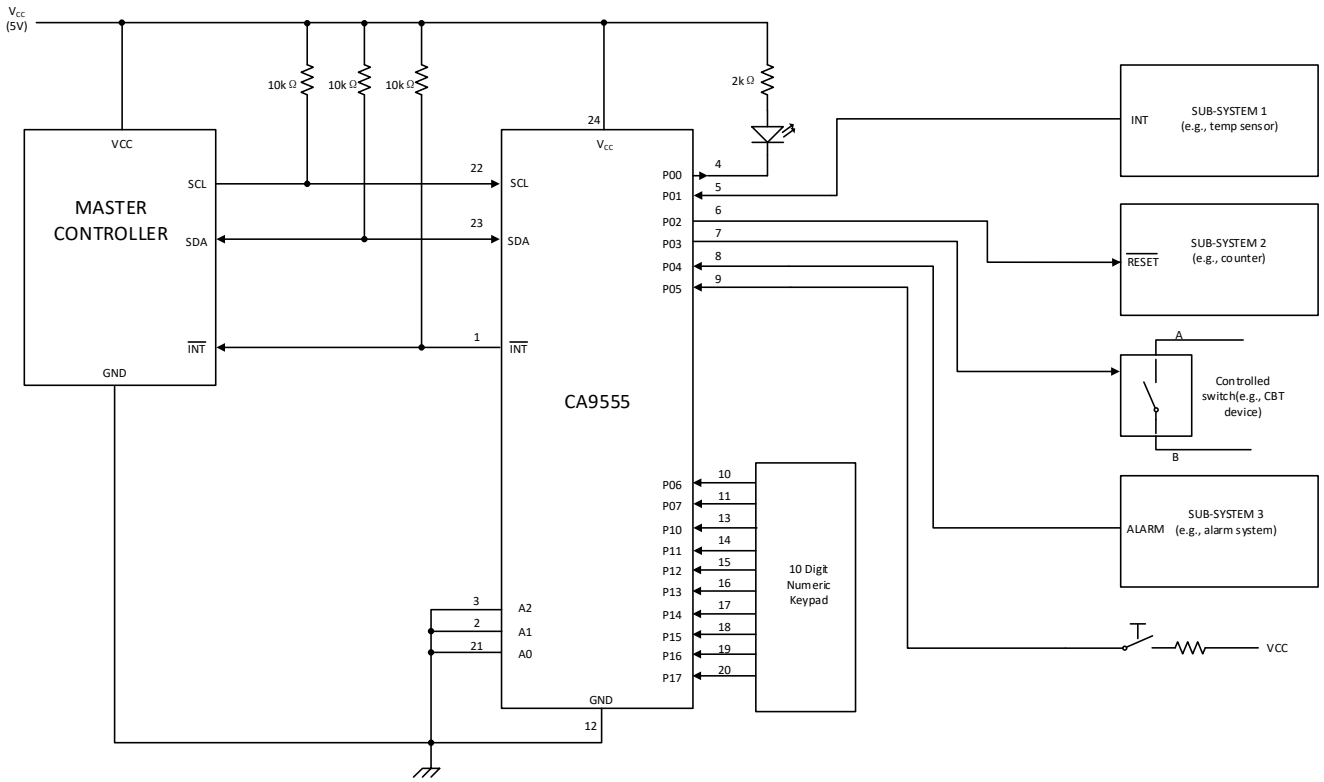


TSSOP-24 (Package Code MT)



QFN4x4-24(Package Code QN)

5. Typical Application



A. Device address configured as 0100 000xb for this example.
B. P00,P02, P03 configured as outputs.
C. P01, P04-P07, and P10-P17 configured as inputs.
D. Pin numbers shown are for the MT package.

Figure 1. Typical Application of CA9555

6. Pin Description

PIN Name	PIN No.		Description
	TSSOP-24	QFN4x4-24	
$\overline{INT}$	1	22	Interrupt output with active low.
A1	2	23	Slave addresses setup pin1, combined with A0, A2, which can generate 8 kinds of slave addresses by connecting these pins to GND or V_{CC} respectively.
A2	3	24	Slave addresses setup pin2, combined with A0, A1, which can generate 8 kinds of slave addresses by connecting these pins to GND or V_{CC} respectively.
P00	4	1	GPIO bit0 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P01	5	2	GPIO bit1 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P02	6	3	GPIO bit2 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P03	7	4	GPIO bit3 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P04	8	5	GPIO bit4 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P05	9	6	GPIO bit5 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P06	10	7	GPIO bit6 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
P07	11	8	GPIO bit7 of Port0, output: push-pull structure; input: internal weakly pull-up structure.
GND	12	9	Ground pin.
P10	13	10	GPIO bit0 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P11	14	11	GPIO bit1 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P12	15	12	GPIO bit2 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P13	16	13	GPIO bit3 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P14	17	14	GPIO bit4 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P15	18	15	GPIO bit5 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P16	19	16	GPIO bit6 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
P17	20	17	GPIO bit7 of Port1, output: push-pull structure; input: internal weakly pull-up structure.
A0	21	18	Slave addresses setup pin0, combined with A1, A2, which can generate 8 kinds of slave addresses by connecting these pins to GND or V_{CC} respectively.
SCL	22	19	Digital interface clock input pin, need a pull-up resistor to V_{CC}.
SDA	23	20	Digital interface data input or output pin, need a pull-up resistor to V_{CC}.
V_{CC}	24	21	Power supply input pin, using 0.1uF low ESR ceramic capacitor to ground

7. Function Block

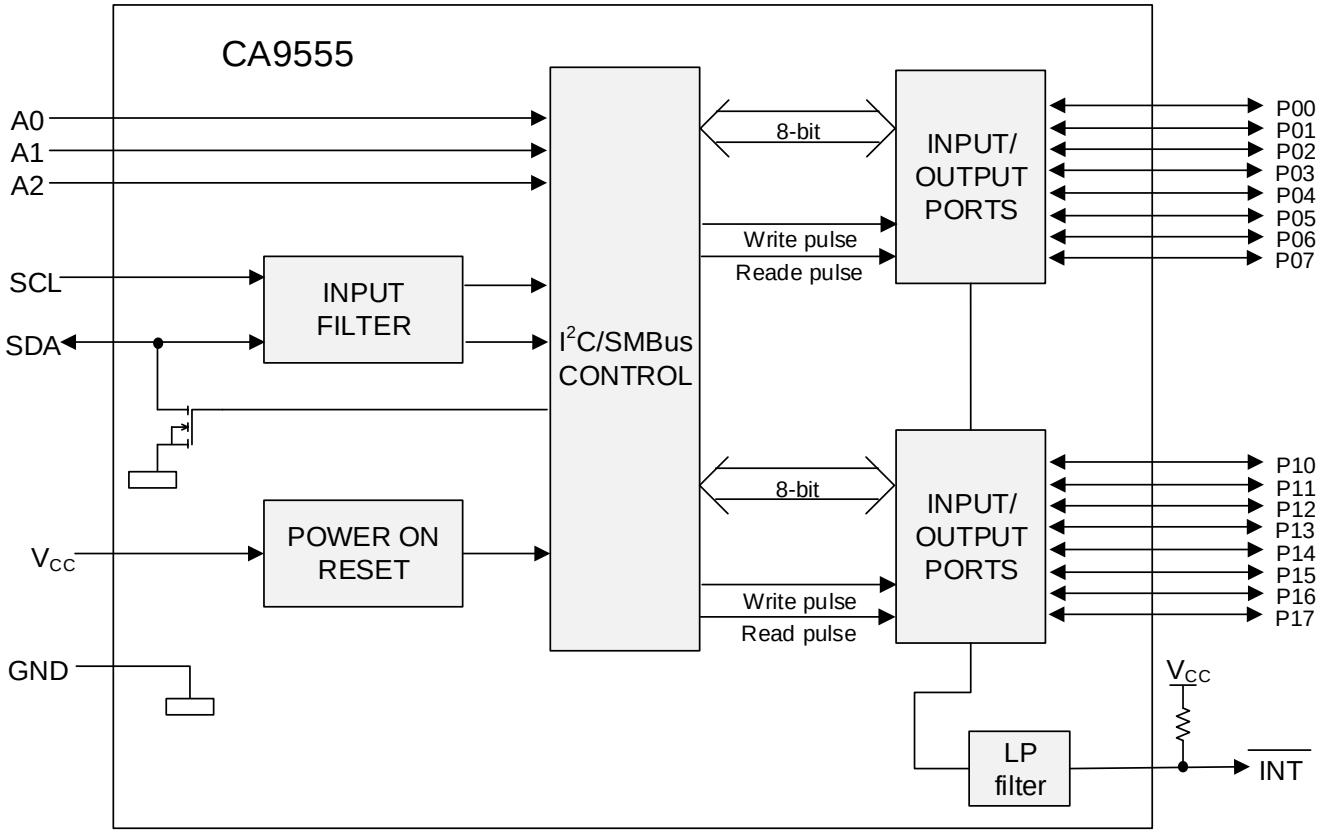
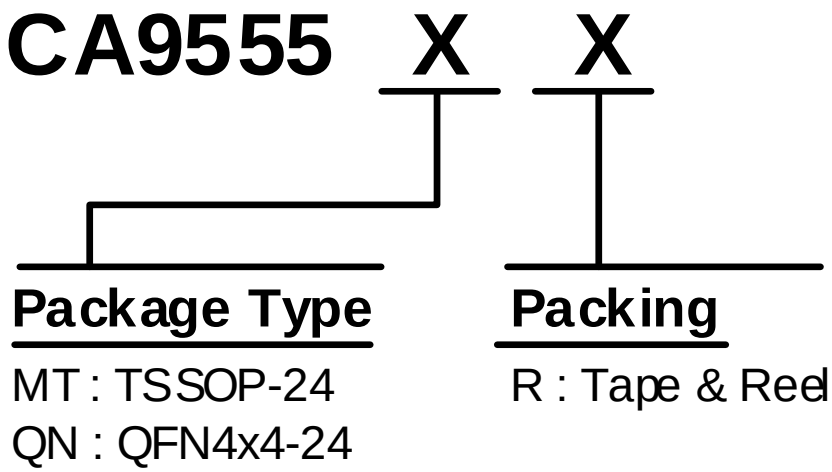


Figure 2. CA9555 function block

8. Ordering Information



Order PN	Green[1]	Package	Marking ID[2]	Packing	MPQ	Operation Temperature
CA9555MTR	Halogen free	TSSOP-24	9555 YWWAXX	Tape & Reel	4,000	-40ºC ~ +85ºC
CA9555QNR	Halogen free	QFN4x4-24	9555 YWWAXX	Tape & Reel	5,000	-40ºC ~ +85ºC

Note

1. Based on ROHS Y2012 spec, Halogen free covers lead free. So most package types Sensylink offers only states halogen free, instead of lead free.
2. Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.

SENSYLINK Microelectronics Inc.

www.sensylink.com

IMPORTANT NOTICE

SENSYLINK Microelectronics Inc. reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein or to discontinue any product or service. Customers should obtain the latest relevant information before placing orders and should verify the latest and complete information. SENSYLINK Microelectronics does not assume any responsibility for use of any product, nor does SENSYLINK Microelectronics any liability arising out of the application or use of this document or any product or circuit described herein. SENSYLINK Microelectronics assumes no liability for applications assistance or the design of Customers' products. Customers are responsible for their products and applications using SENSYLINK Microelectronics components. SENSYLINK Microelectronics does not convey any license under its patent or trademark rights nor the other rights.